Alan Xie

360-228-4453 | US Citizen | axie74@gatech.edu | linkedin.com/in/alanjxie/

Education

Georgia Institute of Technology Atlanta, GA

B.S. Electrical Engineering *Aug. 2025 – May 2028*

- GPA: 4.0 — Threads: Circuit Technology and Signal Processing
- Relevant Coursework: Linear Algebra, Digital Design, Intro to Signal Processing, Object Oriented Programming

Technical Skills

Languages: Python, C++, Java, SystemVerilog,
Software: Git, Altium, LTSpice, Matlab, GNU Radio
Hardware Skills: Oscilloscope, Logic Analyzer, Soldering, Arduino, Teensy
Libraries: NumPy, SciPy, Matplotlib, Sounddevice, Rtlsdr
Clubs & Licenses: Hytech Racing, Amateur Radio Club, Technical Ham Radio License

Experience

Speech Synthesis Engineer May 2026 – Aug. 2026

Neuvoice *Vancouver, WA*

- TBD
- TBD
- TBD

Research? May 2026 – Present

David Anderson's Efficient Signal Processing Lab *Atlanta, GA*

- TBD
- TBD
- TBD

SJ? Oct. 2026 – Present

The Hive Makerspace @ Georgia Tech *Atlanta, GA*

- TBD
- TBD
- TBD

Peer Instructor Sep. 2026 – Present

The Hive Makerspace @ Georgia Tech *Atlanta, GA*

- TBD
- TBD
- TBD

Projects

Self-Made Power Bank Oct. 2025

- Designing PCB with buck-boost, protection, and charger ICs
- Created custom footprints and schematics using Altium
- Currently revising to V2 with C++ firmware for data collection

Software Defined Radio (SDR) Signal Analysis and Demodulation Mar. 2026

- Engineered custom Python scripts for an RTL-SDR pipeline to capture and process FM radio signals at 2.4 MS/s.
- Implemented FM demodulation, filtering, and decimation for real-time signal extraction.
- Built an end-to-end SDR workflow from IQ sampling to audio output with real-time decoding and playback at standard audio rates.

FPGA-Based Digital-to-Analog Converter Apr. 2026

- Built an FPGA-based DAC operating at 100 kHz for real-time digital-to-analog signal generation.
- Applied zero-stuffing upsampling (4× interpolation) with FIR filtering for signal strength and less imaging.
- Implemented and validated timing-critical Verilog modules.